What is claimed is:

1. A memory device with a vertical transistor and a trench capacitor, comprising:

a substrate with at least one deep trench;

a trench capacitor disposed in the bottom of the deep trench;

a conducting wire disposed on the trench capacitor;

a trench top insulating layer disposed on the conducting wire, in which the top trench insulating layer consists of a first insulating layer and a second insulating layer surrounded by the first insulating layer; and

a control gate disposed on the trench top insulating layer.

2. The memory device with a vertical transistor and a trench capacitor of claim 1, further comprising a buried strap in the substrate beside the conducting wire to electrically connect the control gate as a drain.

3. The memory device with a vertical transistor and a trench capacitor of claim 1, further comprising a doped area in the substrate beside the control gate as a source.

4. The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the first insulating layer is an oxide-nitride layer.

5. The memory device with a vertical transistor and a trench capacitor of claim 4, wherein a thickness of the oxide layer is 5 to 10Å.

6. The memory device with a vertical transistor and a trench capacitor of claim 4, wherein a thickness of the nitride layer is 40 to 50Å.

7. The memory device with a vertical transistor and a trench capacitor of claim 4, wherein the oxide layer is formed by thermal oxidation.

8. The memory device with a vertical transistor and a trench capacitor of claim 4, wherein the nitride layer is formed by CVD.

9. The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the second insulating layer is BPSG, PSG, NSG or TEOS oxide layer.

10. The memory device with a vertical transistor and a trench capacitor of claim 1, wherein a thickness of the second insulating layer is 200 to 400Å.

11. The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the second insulating layer is formed by LPCVD.

12. The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the conducting wire has a first conducting layer and a second conducting layer , the conducting wire and the substrate are isolated by a circular insulating layer, and the second conducting layer surrounds the first conducting layer and the circular insulating layer .

13. The memory device with a vertical transistor and a trench capacitor of claim 12, wherein the first conducting layer is a doped poly layer or a doped epi-silicon layer.

14. The memory device with a vertical transistor and a trench capacitor of claim 12, wherein the second conducting layer is a poly layer or a epi-silicon layer.

15. The memory device with a vertical transistor and a trench capacitor of claim 12, wherein the circular insulating layer is a silicon oxide layer.

16. The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the control gate consists of a gate conducting layer and a gate oxide layer, and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof.

17. A method for fabricating a memory device with a vertical transistor and a trench capacitor, comprising:

providing a substrate;

forming at least one deep trench in the substrate;

forming a trench capacitor in the bottom of the deep trench;

forming a conducting wire on the trench capacitor;

forming a trench top insulating layer on the conducting wire, in which the trench top insulating layer consists of a first insulating layer and a second insulating layer surrounded by the first insulating layer; and

forming a control gate on the trench top insulating layer.

18. The method for fabricating a memory device with a vertical transistor and a trench capacitor of claim 17, further comprising a buried strap in the substrate beside the conducting wire to electrically connect the control gate as a drain.

19. The memory device with a vertical transistor and a trench capacitor of claim 17, further comprising a doped area in the substrate beside the control gate as a source.

20. The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the first insulating layer is an oxide-nitride layer.

21. The memory device with a vertical transistor and a trench capacitor of claim 20, wherein a thickness of the oxide layer is 5 to 10Å.

22. The memory device with a vertical transistor and a trench capacitor of claim 20, wherein a thickness of the nitride layer is 40 to 50Å.

23. The memory device with a vertical transistor and a trench capacitor of claim 20, wherein the oxide layer is formed by thermal oxidation.

24. The memory device with a vertical transistor and a trench capacitor of claim 20, wherein the nitride layer is formed by CVD.

25. The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the second insulating layer is BPSG, PSG, NSG or TEOS oxide layer.

26. The memory device with a vertical transistor and a trench capacitor of claim 17, wherein a thickness of the second insulating layer is 200 to 400Å.

27. The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the second insulating layer is formed by LPCVD.

28. The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the conducting wire has a first conducting layer and a second conducting layer , the conducting wire and the substrate are isolated by a circular insulating layer, and the second conducting layer surrounds the first conducting layer and the circular insulating layer .

29. The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the first conducting layer is a doped poly layer or a doped epi-silicon layer.

30. The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the second conducting layer is a poly layer or an epi-silicon layer.

31. The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the circular insulating layer is a silicon oxide layer.

32. The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the control gate consists of a gate conducting layer and a gate oxide layer, and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof.

33. A method for fabricating a memory device with a vertical transistor and a trench capacitor, comprising:

providing a substrate;

forming at least one deep trench in the substrate;

forming a trench capacitor in the bottom of the deep trench;

forming a insulating layer on the trench capacitor, a sidewall of the deep trench, and the substrate;

etching the insulating layer until the insulating layer on the trench capacitor and the substrate is removed to form a circular insulating layer on the sidewall of the deep trench;

filling a first conducting layer in the deep trench;

etching the first conducting layer to expose the circular insulating layer;

etching the circular insulating layer to below the first conducting layer in the deep trench;

forming a second conducting layer on the first conducting layer, the circular insulating layer, the sidewall of the deep trench, and the substrate;

partially etching the second conducting layer to remove the second conducting layer on the sidewall of the deep trench and the substrate to leave the second conducting layer coning the first conducting layer and the circular insulating layer, in which a conducting wire consists of the first conducting layer and the second conducting layer;

conformably forming a first insulating layer on the second conducting layer, the sidewall of the deep trench, and the substrate;

partially etching the first insulating layer to remove the first insulating layer on the second conducting layer and the substrate to form a spacer on the sidewall of the deep trench;

filling a second insulating layer in the deep trench;

etching the second insulating layer to expose the first insulating layer;

etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating layer to leave the second insulating layer on a sidewall of the second insulating layer, in which a trench top insulating layer consists of the first insulating layer and the second insulating layer; and

forming a control gate on the trench top insulating layer.

34. The method for fabricating a memory device with a vertical transistor and a trench capacitor of claim 33, further comprising a buried strap in the substrate beside the conducting wire to electrically connect the control gate as a drain.

35. The memory device with a vertical transistor and a trench capacitor of claim 33, further comprising a doped area in the substrate beside the control gate as a source.

36. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the first insulating layer is an oxide-nitride layer.

37. The memory device with a vertical transistor and a trench capacitor of claim 36, wherein a thickness of the oxide layer is 5 to 10Å.

38. The memory device with a vertical transistor and a trench capacitor of claim 36, wherein a thickness of the nitride layer is 40 to 50Å.

39. The memory device with a vertical transistor and a trench capacitor of claim 36, wherein the oxide layer is formed by thermal oxidation.

40. The memory device with a vertical transistor and a trench capacitor of claim 36, wherein the nitride layer is formed by CVD.

41. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the second insulating layer is BPSG, PSG, NSG or TEOS oxide layer.

42. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein a thickness of the second insulating layer is 200 to 400Å.

43. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the second insulating layer is formed by LPCVD.

44. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the first conducting layer is a doped poly layer or a doped epi-silicon layer.

45. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the second conducting layer is a poly layer or an epi-silicon layer.

46. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the circular insulating layer is a silicon oxide layer.

47. The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the control gate consists of a gate conducting layer and a gate oxide layer, and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof.